

MX0160VP LDMOS TRANSISTOR

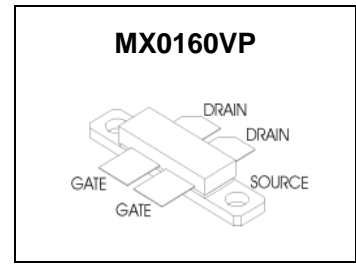
Document Number: MX0160VP
Preliminary Datasheet V1.0

550W, 50V High Power RF LDMOS FETs

Description

The MX0160VP is a 550-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.2 GHz.

It is the thermally enhancement of its peer MK0160VP(S)



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{Ma}$	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current	I_{DSS}	—	—	1	μA

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($V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$)					
Gate--Source Leakage Current ($V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{ V}$, $I_D = 600\ \mu\text{A}$)	$V_{GS(th)}$	—	2.65	—	V
Gate Quiescent Voltage ($V_{DD} = 50\text{ V}$, $I_D = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.25	—	V
Drain source on state resistance ($V_{ds}=0.1\text{V}$, $V_{gs}=10\text{V}$)	$R_{ds(on)}$		217		$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$)	C_{ISS}		208		pF
Common Source Output Capacitance ($V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$)	C_{OSS}		49.6		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$)	C_{RSS}		1.14		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 108\text{ MHz}$, pulse width:100us, duty cycle:10%

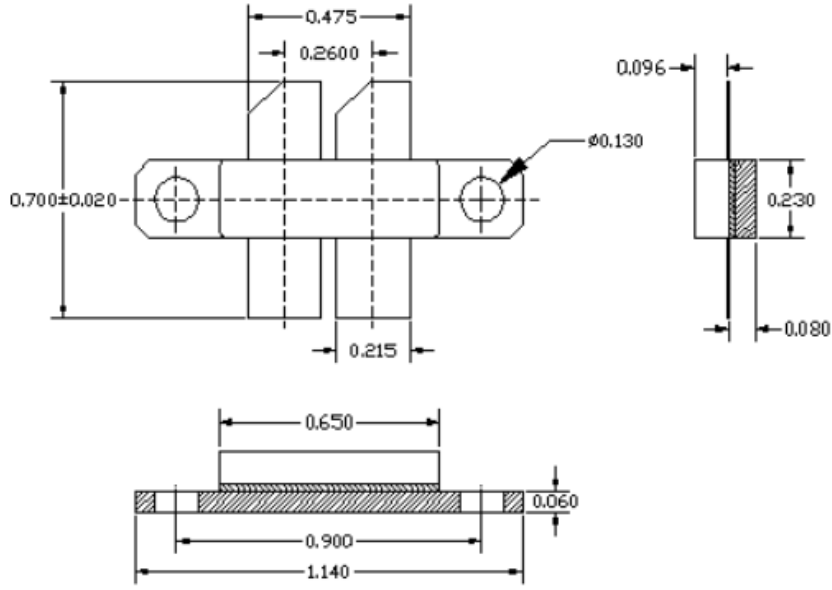
Load 20:1 All phase angles, at 500W Pulsed CW Output Power	No Device Degradation
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Package Outline

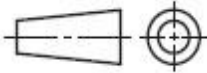
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Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/- .005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/19	Rev 1.0	Preliminary Datasheet Creation

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